For research article

Response to Reviewer 3 Comments

1. Summary

Thank you very much for the careful reading of the manuscript and for the accurate summary of its scope and contributions. We appreciate the detailed and constructive comments. We have addressed all nine points. The corresponding revisions are highlighted in purple in the re-submitted manuscript.

2. Questions for General Evaluation

Questions for General Evaluation	Reviewer's Evaluation	Response and Revisions
Does the introduction provide sufficient background and include all relevant references?	Yes	An explicit problem, goal, idea, novelty and contribution paragraph was added (Comments 1 and 3), plus an FPGA-oriented reference.
Are all the cited references relevant to the research?	Yes	One additional recent reference was added; all remain relevant.
Is the research design appropriate?	Yes	The IEEE-754 limitations and their application-domain impact are now discussed (Comment 5).
Are the methods adequately described?	Can be improved	Equation punctuation and wording were corrected (Comment 2); the 0.f benefits (Comment 4), the MAC/FMA trade-off (Comment 7), and detailed error statistics (Comment 8) were added.
Are the results clearly presented?	Can be improved	The scientific novelty is now explicit (Comment 3) and the limitations of cross-family comparisons are emphasized (Comment 6).
Are the conclusions supported by the results?	Yes	A list of abbreviations was added before the references (Comment 9).

3. Point-by-point response to Comments and Suggestions for Authors

Comments 1: *Please, add the following issues in the Introduction (after the line 83): the problem to be solved, the main goal of the paper, the main idea used by authors to solve the problem, the novelty of the proposed decision, the contribution in the field.*

Response 1: We have added a dedicated paragraph near the end of the Introduction that states these five items explicitly (lines 113 to 129): *The* problem *addressed is the inherent trade-off between hardware-resource utilization and computational performance... The* main goal *is to provide a coherent, parameterizable, and fully portable floating-point unit set... The* main idea*... combines an explicit* $0.f$ *significand encoding... configurable exponent and mantissa widths, and a single VHDL-2008 description... The* novelty *is not a new arithmetic algorithm... The* contribution to the field *is therefore a portable, openly characterized floating-point unit set...* (Line references are to the submitted PDF; the paragraph is placed just before the paper-organization paragraph.)

Comments 2: *Please, show the signs of punctuation after the equations. For example, it should be the sign "." after the formula (4). Also, I think that the expression "AMD (former Xilinx)" should be replaced by "AMD Xilinx" (line 426).*

Response 2: We thank the reviewer for noting that typos. We added the missing terminal punctuation to the display equations that close a sentence, including the period after Eq. (4) [$R = (A \times B) + C.$] and commas after Eq. (3), the energy-per-operation equation, and the ATP equation. We also replaced both occurrences of "AMD (formerly Xilinx)" by *"AMD Xilinx"* (lines 105 and 517).

Comments 3: *The scientific novelty should be clarified more explicitly. The manuscript primarily integrates known techniques into a coherent framework rather than introducing fundamentally new arithmetic algorithms.*

Response 3: We fully agree, and we have made this explicit in the new Introduction paragraph that also answers Comment 1 (lines 122 to 129): *the novelty is not a new arithmetic algorithm: the units integrate known techniques into a coherent, portable framework and are characterized under a uniform area-equivalent metric across two FPGA generations...* consistent with the contribution paragraph, which states that the work consolidates a coherent and portable unit set rather than proposing a novel arithmetic algorithm.

Comments 4: *The benefits of the proposed 0.f significand representation are discussed mainly qualitatively. Additional quantitative evidence isolating its contribution to area, timing, and power savings would strengthen the paper.*

Response 4: We have strengthened Section 3.1 by expanding the structural argument (which corner-case multiplexers and control the 0.f encoding removes) and by clarifying quantitatively that the encoding is precision-lossless, corroborated by the numerical validation (lines 312 to 335, also responding similar comments from other reviewers). A clean isolation of the area, timing, and power contribution requires a functionally equivalent 1.f re-implementation, which we do not currently have. We have therefore identified this direct 1.f-vs-0.f synthesis comparison as future work rather than report unsubstantiated numbers.

Comments 5: *I think that the proposed units are not fully IEEE-754 compliant. For example, NaN, infinity, denormalized numbers, and multiple rounding modes are not supported. The impact of these limitations on potential application domains should be discussed more thoroughly.*

Response 5: We agree. In addition to the clarifications that the format is IEEE-754-inspired but not fully compliant, we have added to Section 3.2 a discussion of the application-domain impact of these limitations (lines 362 to 375): *They are immaterial for the streaming DSP datapaths targeted here... Conversely, the omitted features do matter for: general-purpose or library-grade floating-point that must propagate NaN/*$\pm\infty$*... algorithms that depend on gradual underflow... and applica-*

tions requiring directed rounding, such as interval arithmetic... For such domains the compatibility wrapper and additional rounding logic would be required, with the corresponding overhead.

Comments 6: *Several comparisons involve designs implemented on different FPGA families and process technologies. The authors should further emphasize the limitations of such comparisons and discuss their effect on the conclusions.*

Response 6: We agree, and we have strengthened the cross-technology item in Section 4.1 to state the effect on the conclusions explicitly (lines 588 to 600): *comparisons spanning different process nodes... must be read as indicative of architectural and resource-efficiency trends, not as absolute frequency or power superiority... the strongest and most controlled evidence for the headline ATP claims comes from the same-device, same-node comparisons... on the Kintex UltraScale (20 nm) part, where the area-equivalent metric, the operating frequency, and the power-estimation flow are identical for all designs.*

Comments 7: *The MAC unit is implemented as a non-fused architecture. A deeper comparison with fused multiply-add (FMA) alternatives would be valuable, particularly regarding numerical accuracy and latency.*

Response 7: We have deepened this comparison in the MAC discussion along both axes (lines 712 to 721). On accuracy, the non-fused chained design has a worst-case error of 1 ULP versus the 0.5 ULP of a fused operator (single final rounding). On latency, we added: *The non-fused MAC has a latency equal to the sum of the multiplier and adder pipelines (8 cycles)... A fused multiply–add merges the two normalization/rounding stages into one, which both removes the intermediate rounding... and shortens the datapath by one normalization stage...* The non-fused choice trades one extra rounding and one extra normalization stage for the modularity of reusable multiplier/adder blocks; a full FMA characterization is part of the future work.

Comments 8: *The numerical validation section should include more detailed statistical results and error distributions to provide stronger evidence of correctness.*

Response 8: We agree and thank the reviewer for noting that point, and we have added statistical results to the Numerical Validation section (lines 791 to 804, table 6 and figure 7): a new table reports the mean, RMS, and maximum operator-induced error (in ULP) over the two 5,000-vector campaigns, and a new figure shows the error distributions. The multiplier and adder errors are confined to $[0, 0.5]$ ULP (mean ≈ 0.25 ULP, RMS ≈ 0.29 ULP); the chained MAC stays at or below 1 ULP in the common $|P| \leq |R|$ regime (mean ≈ 0.28 ULP). We also report transparently that *the complementary cases, in which the addend nearly cancels the product ($|P| > |R|$, about 22–27% of the random vectors), exhibit a larger relative error... exactly as predicted by the chained-rounding analysis...* which both strengthens the evidence of correctness and further motivates the FMA variant discussed in Comment 7.

Comments 9: *Please, add the list of used acronyms before the section "References". This is the must for Electronics.*

Response 9: Done. An Abbreviations list has been added in the back matter before the References.

4. Response to Comments on the Quality of English Language

Point 1: The reviewer indicated that the English does not require improvement.

Response 1: We thank the reviewer. The newly added text was written consistently with the existing style of the manuscript.

5. Additional clarifications

All revisions made in response to the comments above are highlighted in purple in the re-submitted manuscript (the equation-punctuation fixes, tables and figures and the Abbreviations list are structural edits and are not colored). We thank the reviewer again for the thorough and constructive feedback.