Authors' Response to Comments

We thank the reviewers and the Editor for their valuable comments, which have helped us to greatly improve our manuscript. Please find below our point-by-point responses and other revisions we made. To facilitate the reviewing process, here we use red texts to indicate the revisions and blue texts to indicate their locations in the revised manuscript.

General Comments:

The paper deals with the design of a novel algorithm based on simulated annealing to solve DRC violations in integrated circuits. The algorithm was tested both on standard mosfet in 28nm and FinFET devices in 14nm, showing the possibility to solve layout violations in acceptable amount of time.

Reply: We thank the reviewer for the positive comments.

The following points are highlighted:

Q1 *Section 2.2.1 immediately starts with a description of the work objective without giving details about the simulated annealing algorithm. I suggest adding an introduction to this algorithm, specifying the meaning of "temperature" and "temperature decay" concepts in this context. This will help also readers not used to this topic to understand the proposed method.*

Reply: We thank the reviewer for pointing this out. We added explanations for "temperature" and "temperature decay" in the manuscript:

"In standard cell layout restoration, the objective is to have conflicts between graphics minimized and to ensure that the distances between all graphics are made to meet user-defined minimum distance constraints. During the algorithm's operation, there will first be an inferior solution, which refers to the solution with a higher objective function value and more severe conflicts between graphs. Such solutions are usually accompanied by an intensification of DRC violations. For instance, suppose that there is an irregular spacing of metal wires in a certain layout (the actual spacing is 3 nm, which is less than the 5 nm required by the design rule). Through Equation (1), the objective function value of the algorithm in the current state can be calculated as $E_1 = 4$.

$$E = \sum \max(0, d_{\min} - d_{ij})^2 \quad (1)$$

If the algorithm generates a new state, causing the metal wire spacing to further reduce to 2 nm, at this time the objective function value becomes $E_2 = 9$. This new state is an inferior solution, with more severe DRC violations and a higher objective function value. It is a solution that is not helpful for repairing the objective (eliminating DRC violations) or even has a counterproductive effect. Therefore, traditional simulated annealing algorithms will accept such inferior solutions with a certain probability, with the aim of avoiding getting trapped in local optima [19-20]. For instance, if there are still unrepaired errors near the current optimal solution, it is necessary to accept the inferior solution to break out of the local area and explore a better repair direction. The

improved simulated annealing algorithm, through an adaptive temperature attenuation strategy, dynamically adjusts the probability of accepting an inferior solution, thereby more efficiently balancing global exploration and local convergence, and focusing on the optimal repair result. Among them, temperature refers to the control parameter T set by the algorithm in each round of iteration, which determines the probability of the algorithm accepting inferior solutions. The higher the temperature, the greater the probability of accepting the inferior solution, which is conducive to breaking away from the local optimum. The lower the temperature, the smaller the probability of accepting inferior solutions, and the algorithm tends to converge. Temperature decay, on the other hand, refers to the mechanism by which temperature gradually decreases during an iterative process, which is used to simulate the cooling stage in the physical annealing process. By reasonably setting the temperature attenuation strategy, the global exploration and local development capabilities of the algorithm can be balanced, and the convergence efficiency and the quality of the solution can be improved.

Therefore, the proposed improved simulated annealing algorithm adopts an adaptive temperature decay strategy to dynamically adjust the temperature decay coefficient based on the quality of the current solution and the number of iterations of the search, in order to better automatically repair DRC errors in standard cells." (Pages 3 to 4, lines 94 to 130)

Q2 *Define also the meaning of "conflicts" in the point (2) of line 147.*

Reply: We thank the reviewer for pointing this out. We added explanations for "conflicts" in the manuscript:

"Calculate the number of conflicts between each graphic and other graphics. In a standard cell layout, a conflict refers to the situation where the geometric distance d_{ij} between any two figures i and j is less than the minimum spacing constraint d_{min} given by the user. Each time this situation occurs, the respective conflict counters increase by 1. Then sort the graphics in descending order of conflict frequency. In the generation of neighborhood solutions, priority is given to selecting graphics with more conflicts for position adjustment to generate new solutions x'. For example, add a random small offset to the x and y coordinates of the graph with the highest number of conflicts, such as a random number between [-0.1, 0.1]." (Page 5, lines 174 to 182)

Q3 *Please, organize section 2.2.2 adding more references to Fig. 2. Also the mathematical details of the algorithm should be collected in a dedicated flow chart to enhance comprehension. Try to improve also the graphic quality of Fig. 2 (the image is stretched, and some labels are not within their boxes).*

Reply: We thank the reviewer for pointing this out. We have already revised Figure 2 in the manuscript:

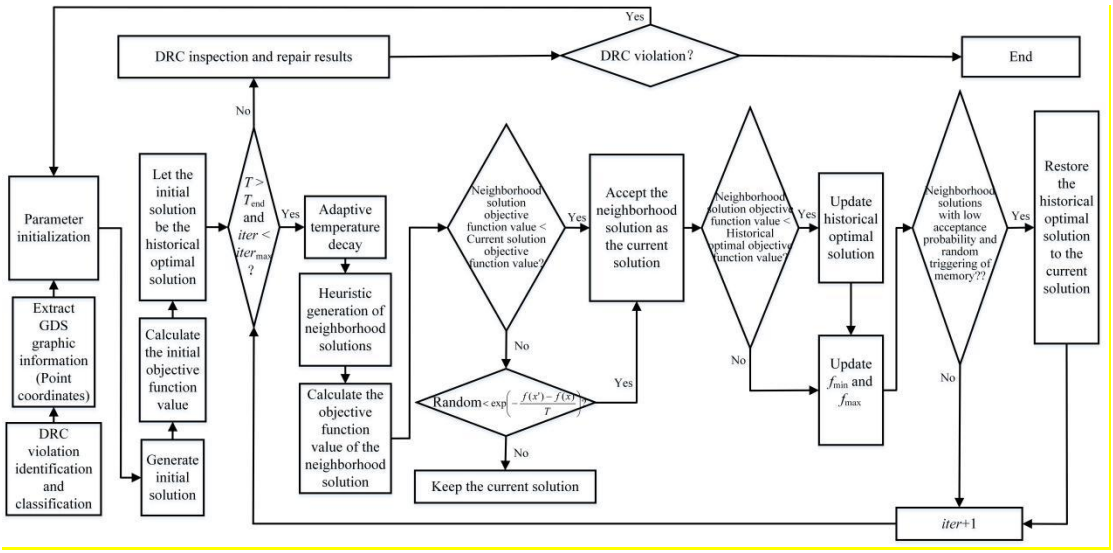

Figure 2. Algorithm flowchart.

Q4 *In the result section, please add information about the computer/server used to verify the algorithm, specifying the king of CPU, frequency, amount of memory, operative system etc. Specify also how you verify the absence of violations after the algorithm (is the final verification with Calibre?).*

Reply: We thank the reviewer for pointing this out. We have added information about the computer/server details for verifying the algorithm in the results section of the manuscript:

"To verify the effectiveness and feasibility of the proposed DRC automatic repair method, a series of experiments were designed. And it runs on a Windows operating system with a CPU of 11th Gen Intel(R) Core(TM) i7-11700K and a frequency of 3.60GHz. Standard cell layouts in the 28 nm MOSFET process and 14 nm FinFET process were utilized for DRC violation repair." (Page 7, lines 238 to 242)

And we also explained that after the proposed method was repaired, Calibre was used for the final verification to ensure there were no DRC violations in the results section of the manuscript:

"After the proposed method is repaired, the industry standard tool Calibre is used to check the design rules to ensure that there are no violations, thereby guaranteeing that the layout fully complies with the design rule requirements." (Page 9, lines 328 to 330)

Q5 *The proposed work is mainly focused on the solution of spacing problems. However, other kinds of DRC violations demand for suitable care, like enclosure, latch-up, antennas etc.. Is there the possibility of extending this work also to the solution of these violations? I believe it is important to add some considerations about this part in the text.*

Reply: We thank the reviewer for pointing this out. For DRC violations that are enclosure and latch-up, they essentially fall under the category of spacing problems, and the proposed methods can solve them. However, the DRC problem of the antennas effect is not within the scope of

discussion of the proposed method, as this violation is a special electrical performance violation problem that requires the addition of components to be resolved.

Q6 *It is suggested to add the following examples of integrated circuits to highlight the importance of solving DRC errors in handcrafted layouts while preserving electrical performance. This also help improve the literature contextualization of the paper in the realm of integrated circuit design:*

Tegazzini, G. Di Meo, D. De Caro and A. G. M. Strollo, "High-Precision MUX-Based Digital Delay Interpolators Based on a Novel Transistor Sizing Algorithm," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 7, pp. 938-942, July 2025, doi: 10.1109/TCSII.2025.3571482.

Marinberg, E. Garzón, T. Noy, M. Lanuzza and A. Teman, "Efficient Implementation of Many-Ported Memories by Using Standard-Cell Memory Approach," in IEEE Access, vol. 11, pp. 94885-94897, 2023, doi: 10.1109/ACCESS.2023.3310940.

Reply: We thank the reviewer for pointing this out. We have added the two references in the manuscript:

"The standard cell library serves as an important bridge for digital integrated circuits, and the layout design in its construction process is regarded as the most complex and time-consuming task [1]. This is mainly because the layout design has to adhere to extremely complex design rules, which are interdependent and interrelated [7]. " (Page 1, lines 30 to 34)

And the references listed in the manuscript:

"1.Marinberg H, Garzón E, Noy T, et al. Efficient implementation of many-ported memories by using standard-cell memory approach[J]. IEEE Access, 2023, 11: 94885-94897. (Page 11, lines 378 to 379)

7.Tegazzini L, Di Meo G, De Caro D, et al. High-Precision mux-Based Digital Delay Interpolators Based on a Novel Transistor Sizing Algorithm[J]. IEEE Transactions on Circuits and Systems II: Express Briefs, 2025. (Page 11, lines 408 to 409)"