

Reviewer Responses for Sensors-3773983

Dear Sirs/Madams,

We sincerely appreciate the Editor-in-Chief, Associate Editor, and reviewers for their time and effort in reviewing our manuscript. Thank you for allowing us to address the reviewers' comments and resubmit our manuscript. We have carefully considered the reviewers' comments and suggestions from the previous submission.

Title: *An Overview of Phase-Locked Loop: From Fundamentals to the Frontier*

Authors: *Thi Viet Ha Nguyen and Cong-Kha Pham*

We are uploading (a) our point-by-point response to the comments (below), and (b) an updated manuscript with yellow highlighting indicating new contents, rephrased sentences, and new references.

With our efforts and changes, we hope that the updated manuscript will qualify for publication in this journal. We would be glad to respond to any further questions or comments you may have. We are looking forward to hearing from you regarding our manuscript.

Best regards,

Thi Viet Ha Nguyen *et al.*

2. Reviewer #3

2.1. Concerns #3

The contribution of this work should be motivated with respect to other reviews by referencing the papers you're taking as comparison, and discussing the differences with respect to each of them. Moreover, the research strategy to build up this review is completely missing.

Author response: Thank you for your valuable feedback. Compared to the referenced surveys, our review is superior in addressing modern PLL challenges through explicit, justified contributions:

- Unlike earlier works that focus on analog/digital shifts or fractional-N purity, we introduce a novel framework evaluating PLL architectures (e.g., APLLs, DPLLs, ILPLLs, etc.) specifically for low-power emerging applications, enabling designers to balance energy efficiency with metrics like phase noise and jitter.
- This work provides an in-depth analysis of recent design techniques, especially for IoT and mmWave applications, which have not been explored in previous reviews.
- We deliver actionable guidance on phase noise, jitter, spurs, and digital calibration, supporting next-generation designs extending beyond the theoretical or circuit-level focus of the compared works.

To motivate this review's contributions, we compare it to three key PLL surveys, highlighting differences in scope, focus, and coverage to address gaps in emerging applications like IoT and mmWave systems.

- Razavi (1996): Focuses on analog PLL fundamentals and loop dynamics, without addressing digital architectures or low-power/mmWave needs. Our review expands to DPLLs/ADPLLs and recent ML-assisted approaches.
- Staszewski et al. (2005): Introduces early all-digital PLLs for mobile, but underemphasizes ultra-low-power methods or mmWave considerations. We address these with adaptive bandwidth and calibration for IoT/5G+.
- De Muer & Steyaert (2003): Targets CMOS fractional-N synthesizers for spectral purity but omits broader applications. We extend the discussion to jitter, spurs, and calibration across architectures for modern systems.

Author action: We have improved and clarified the motivation of our work with respect to other reviews by referencing and discussing the differences among key papers in *Section 1 (Introduction)*, specifically in paragraphs 3 and 4 (lines 26–48).

2.2. Concerns #5

Your aim should be clarified in the text.

Author action: Thank you for your comment. We have introduced clarification on the reason for the year-by-year timeline arrangement, which aims to support readers especially those new to the field in easily grasping the pace of development, tracking technological trajectories, and connecting innovation milestones with broader trends, such as low-jitter design (phase noise reduction), hybrid analog-digital integration, and energy efficiency, thereby enhancing the usefulness and accessibility for readers. We have clarified this in *Section 2 A Brief History - A Journey Through Time* in paragraph 1 from line 67 to 79.

2.3. Concerns #6

Not answered.

Author action: Thank you for your comment. We acknowledge that the initial submission contained a limited number of references in the system-level description section. In the revised manuscript, we have substantially expanded the literature review to include both foundational and recent works. Specifically:

- Basic frame and System model: Added classic references such as Razavi (1996), De Muer & Steyaert (2003), and Murthi (1979).

Classification of PLL Architectures: Each architecture type is now supported by multiple representative references:

- APLL: Razavi (1996); Murthi (1979).
- Digital DPLL: Kong et al. (2016); Liu et al. (2018); Park et al. (2021); Dartizio et al. (2025).
- All-Digital PLL: Staszewski et al. (2005); Ho & Chen (2016); Wu et al. (2017); Cherniak et al. (2018).
- Integer PLL: Kong et al. (2016); Jo et al. (2023).
- Fractional PLL: Seong et al. (2020); Park et al. (2021); Wu et al. (2021); Gao et al. (2016).
- Injection-Locked PLL: Zhang et al. (2019).

- Delay-Locked Loop: Liu et al. (2021); Huang et al. (2016).

These additions ensure that the section now captures both historical context and state-of-the-art advances, providing a more complete and balanced system-level perspective.

Author action: We updated the manuscript by adding various references. These changes are highlighted in the reference in *Section 3 System View*.

2.4. Concerns #7

In DPLLs PFD is usually substituted by a TDC since the PFD (in its original form, if you are referring to it) produces an output that is used to drive a charge pump analog circuit. Please clarify this aspect.

Author action: Thank you for your insightful comment. We acknowledge that in fully digital PLLs (DPLLs), the conventional Phase-Frequency Detector (PFD) is typically replaced by a Time-to-Digital Converter (TDC), as the original PFD output drives an analog charge pump circuit which is not present in DPLLs. To clarify this aspect, we have revised the manuscript to explicitly state that the figure illustrates the general phase detection concept, while in practical DPLLs, the phase detection function is performed by a TDC to maintain a fully digital loop architecture. This clarification can be found in *Section 3 System View, from line 437 to line 444*.

2.5. Concerns #8

There are more recent publications addressing adaptive DDS-PLL beamsteering architectures operating in real-time.

Author action: Thank you for your valuable suggestion. We have updated the manuscript by including recent and relevant publications on adaptive DDS-PLL beamsteering architectures operating in real-time. Specifically, we have cited the recent works by Avitabile et al. (ISOC2024), Florio et al. (MWSCAS2024), Florio et al. (SpliTech2024), and Karim and Ali (DSP2023). These additions ensure our review reflects the latest advancements in *Section 6 Future Trends in PLL Design, part 6.3. Wideband, Fast-Locking and DDS-Based PLLs for Next-Generation Communications*.

2.6. Concerns #9

Misc: references 68-69 are duplicated.

Author action: Thank you for pointing out the duplication of references 68 and 69. We have carefully reviewed the bibliography and removed the duplicate entry to ensure all references are unique. The updated reference list reflects this correction.