Response to Reviewer 1 Comments

1. Summary

Thank you very much for taking the time to review this manuscript. Please find the detailed responses below and the corresponding revisions in the re-submitted files.

2. Questions for General Evaluation	**Reviewer's Evaluation**	**Response and Revisions**
Does the introduction provide sufficient background and include all relevant references?	Must be improved	
Are all the cited references relevant to the research?	Must be improved	
Is the research design appropriate?	Can be improved	
Are the methods adequately described?	Can be improved	
Are the results clearly presented?	Must be improved	
Are the conclusions supported by the results?	Can be improved	

3. Point-by-point response to Comments and Suggestions for Authors

Comments 1: The authors have already pointed out that the use of jfet to reduce current noise in front-end circuits is a more mature scheme, and the authors should describe what is innovative about the work in this paper? What are the advantages of the results of this paper compared with the peers? Why didn't you use the low current noise op-amps such as LTC6268?

Response 1: Thank you very much for your suggestions on the manuscript. The use of jfet in front-end circuits to reduce current noise may be a relatively mature scheme, but different problems will occur for circuits with different applications. In the early stage of development, we carried out the optimization and comparison experiment of the transformer. During the experiment, due to the large noise contribution of the non-discrete TIA circuit, the noise of the optimized transformer was completely submerged in the noise of the TIA, and its optimization effect was not well reflected.

The innovation of this paper is to sum up the problems encountered in the engineering practice. Therefore, this paper summarizes the noise contribution of transformer noise and TIA circuit, and explains the relationship between them. In this paper, the transformer with higher Q value is used to reduce the transformer noise, and JFET is used as the input stage to reduce the TIA circuit noise. The proportion of noise reduction is calculated theoretically and verified experimentally. The influence of feedback resistance and feedback capacitance on TIA noise is further analyzed. It is pointed out that increasing the feedback resistance can reduce

the noise of the discrete TIA circuit, but in conjunction with the inherent noise of the transformer, the reduced TIA noise can't be well reflected, and the noise contribution of the transformer in the capacitive sensing circuit is approximately 80%. Thank you very much for your suggestions. We have revised the description of the introduction and conclusion in the manuscript for the innovation of this paper. (Page2, L88 and Page15, L378)

At the same time, this paper mainly reflects the development progress of capacitive sensing circuit in Taiji project. Compared with the previous capacitive sensing circuit, the resolution of capacitive sensing is reduced from 1.095aF/rtHz@10mHz to 0.84aF/rtHz@10mHz.

Compared with other research results, this paper focuses on the restriction relationship of circuit noise, and further analyzes the influence of TIA feedback resistance and feedback capacitance on its noise. The theoretical noise of different transformers and before and after using discrete TIA is calculated and verified. For capacitive sensor resolution, there are no public and unified data processing methods reported at present, and compared with the previous scheme, the improvement of capacitive sensor resolution can prove the advantages of this optimization scheme.

Thank you very much for your suggestion on using the LTC6268 low current noise op amp. We did not use a better performance op amp because the performance impact of the op amp is no longer important after using the discrete TIA solution. The use of discrete TIA can make the selection range of operational amplifiers wider, for engineering and aerospace considerations, which makes subsequent screening of devices that meet aerospace requirements easier. For ground experiments, we do not deny that LTC6268 is also one of the effective ways to reduce TIA circuit noise. We will try and study your suggestion in the subsequent experiments.

Comments 2: Is the noise modeling of a discrete jfet front-end circuit correct? The input voltage noise and input current noise of the op-amp will be induced to the gate through the gate source capacitance of the jfet. In Table 4 about each noise calculation and noise factor, the voltage and current noise of the op-amp does not flow directly through the feedback loop, why is the noise gain also NG?

Response 2: Thank you very much for your comments. According to your question, we have re-checked and confirmed the correctness of the noise modeling of the discrete jfet front-end circuit. Table 4 is quoted from literature [17]. In order to display the content related to noise calculation more clearly, the content in the table is simply optimized.

In Figure 5, the power supply end is short-circuited to ground for noise analysis. As you said, the current and voltage noise of the op amp will be induced to the gate through the gate-source capacitance of the jfet. The voltage noise induced to the grid is the op-amp voltage noise, and the current noise induced to the grid is the voltage noise that will be converted to $i_{AMP}r_{DS}$. They are finally induced to the op amp output through a feedback loop, in which the noise gain of the feedback loop is NG.

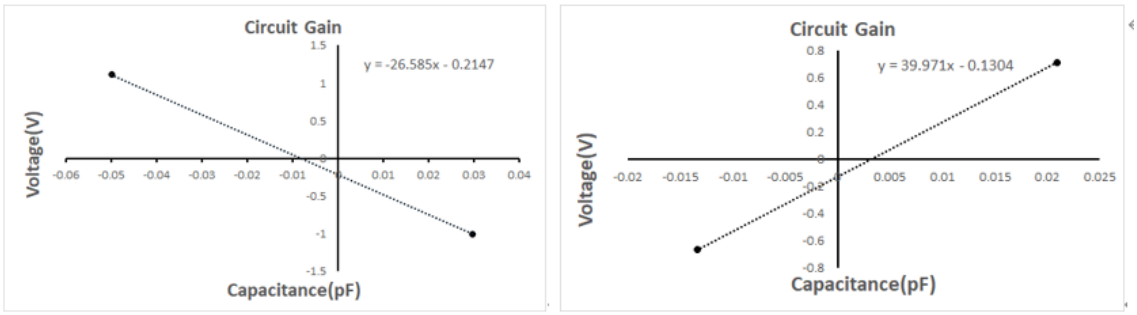
Comments 3: Why is the Driving Capacitance value in Table1 at the pF level?

Response 3: Thank you very much for your question. This is an undeserved error, we have re-examined the parameters of the full text and modified the drive capacitance to 10nF. (Page4,

Line135, Table 1)

Comments 4: What is the amplitude of the carrier wave? There is a lack of circuit related gain calibration tests.

Response 4: The carrier amplitude is 1.2Vp, related instructions are added to Page13 Line345. Circuit gain test results are supplemented with section 4.3.(Page12, Line335 and Figure 12)



(a) (b)

Figure 12. (a) The non-discrete TIA circuit gain test result is 26V/pF, (b) Discrete TIA circuit gain test result is 40V/pF.

Comments 5: What is the purpose of the section of 3.1.3?

Response 5: This section mainly describes the problem of source resistance selection encountered in the test process. During the experiment, improper source resistance will make the circuit work abnormally, so the selection method of source resistance is summarized in this section. The content of this section is not relevant to the test of circuit noise analysis and capacitance sensing resolution. After full discussion by team members, the content of this section is deleted according to your suggestion.

Comments 6: The authors do not give experimental data curves for the tuning noise of the separated front-end circuit, similar to Figure3, to illustrate the percentage of the contribution of other noises such as transformer thermal noise, jfet, op-amps, etc. in the new scheme. Does the tuned output noise of the front-end circuit agree with the theoretical calculation?

Response 6: Thank you very much for your suggestion. According to your suggestion, we added the noise contribution percentage of different transformers before and after using discrete TIA to illustrate the restrictive relationship between transformer noise and TIA noise in capacitive sensing circuits. (Page11, Line298 and Figure 9)

In addition, the paper has given the test results of different transformers (Figure 10), the test results of TIA circuit noise before and after JFET optimization, (Figure 11), and the comparison of the test results of the final capacitance sensing resolution (Figure 14).

Since the equivalent noise of the transformer cannot be measured, the equivalent noise difference of different transformers is 10% (Page12, Line310) according to the theoretical calculation. According to the noise test results of different transformers in Figure 10, the final output noise is reduced by about 11%, which is basically consistent with the theoretical calculation.

The difference in TIA noise theory before and after using discrete JFET optimization is 85%(Page12, Line330), and the final test results show that the difference is about 83%(Figure 11). The test junction can show the effectiveness of using JFET to optimize TIA.

There is a certain error between the final output noise of capacitive sensing and the theoretical calculation, which is caused by electromagnetic interference in the test environment, temperature change and non-independent grounding environment. In the same test environment, using the theoretical calculation difference and the actual test difference to verify each other can exclude the common mode influence caused by other factors such as the test environment, and can show the consistency of the theoretical calculation and the actual test results.

4. Response to Comments on the Quality of English Language

We have looked for a professional team to polish the full text.

5. Additional clarifications

Reviewer 1 Point： The work lacks originality, which is similar to the paper named "Development of Electronic System for Sensing and Actuation of Test Mass of the Inertial Sensor LISA". The authors need to clarify the innovative and the contribution.

Response: As I expressed in comments 1, the innovation and contribution of this paper is to reflect the development of capacitive sensing circuits in the Taiji project. Through the practical problems encountered in the development of capacitive sensing circuit, this paper summarizes the noise contribution of transformer and TIA circuit, and explains the relationship between them. In this paper, the transformer with higher Q value is used to reduce the transformer noise, and JFET is used as the input stage to reduce the TIA circuit noise. The proportion of noise reduction is calculated theoretically and verified experimentally. The influence of feedback resistance and feedback capacitance on TIA noise is further analyzed. It is pointed out that increasing the feedback resistance can reduce the noise of the discrete TIA circuit, but in conjunction with the inherent noise of the transformer, the reduced TIA noise can't be well reflected, and the noise contribution of the transformer in the capacitive sensing circuit is approximately 80%. Compared with the previous capacitive sensing circuit, the resolution of capacitive sensing is reduced from 1.095aF/rtHz@10mHz to 0.84aF/rtHz@10mHz.

Thank you very much for your suggestions. According to your suggestions, we have re-optimized the introduction and conclusion of the article. (Page2, L88 and Page15, L378)

The paper named "Development of Electronic System for Sensing and Actuation of Test Mass of the Inertial Sensor LISA" is an excellent capacitive sensing circuit design solution. Different from the literature, this paper summarizes the relevant progress of Taiji project and the problems encountered on the basis of it, further verifies the theoretical calculation results of transformer noise and TIA noise before and after discrete through practical tests, and further analyzes the influence of feedback resistance and feedback capacitance in TIA noise on TIA noise. At the same time, this paper also provides a different analysis of the parameter Rds.